REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1, 15, and 28-29 have been amended. Claims 1 and 4-29 are pending and under consideration.

Applicants have timely filed a Request for Continued Examination (RCE) along with this Amendment, including the filing fee as set forth in 37 CFR 1.17(e). Accordingly, Applicants respectfully request that the Examiner withdraw the finality of any Office action and enter this Amendment for consideration under 37 CFR 1.114.

I. Rejections under 35 U.S.C. § 103

In the Office Action, at pages 2-8, numbered paragraphs 3-14, claims 15-17, 19-25, and 29 were rejected under 35 USC § 103(a) as being unpatentable over Yamada (U.S. Patent No. 5,950,222) in view of Iwata (U.S. Patent No. 5,881,295).

The Examiner concedes that Yamada does not disclose a conversion circuit. Specifically, Yamada does not discuss or suggest "a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag to convert the first address range to the second address range," as recited in claim 15 as amended. The Examiner seeks to make up for this deficiency with reference to the address conversion circuit of Iwata (Iwata, col. 14, lines 6-15; Fig. 5). However, Iwata does not discuss or suggest "a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag to convert the first address range to the second address range," as recited in claim 15. In other words, the invention of claim 15 provides for converting the first address range *corresponding to the first storage area* to the second address range *corresponding to the second storage area* upon detection of a flag indicating that the first storage area is not accessible, wherein both storage areas are *nonvolatile* storage areas within the nonvolatile memory. As such, the registers of the invention of claim 15 are provided for converting a first address range to a second address

range. In contrast, the address conversion circuit of Iwata provides for converting the address signal for accessing the vector address storage A-V into the address signal for accessing the vector storage address area B-V, where vector address storage A-V is located in a non-volatile built-in ROM and vector address storage B-V is located in a *volatile built-in RAM.* Therefore, it is respectfully submitted that the Examiner has incorrectly concluded that vector address storage area B-V is analogous to the second address range, as one skilled in the art would readily appreciate the difference between a non-volatile storage area and a volatile storage area. Furthermore, the program/erase control register and the erasing0block designation registers of Iwata are used by the control circuit for erasing or programming the flush memory (Iwata, col. 24, lines 15-18). Iwata makes no mention of pairing the registers and setting an address range to each pair, as is provided by the invention of claim 15.

Since neither Yamada nor Iwata discusses or suggests "a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag to convert the first address range to the second address range," as recited in claim 15, claim 15 patentably distinguishes over Yamada and Iwata. Accordingly, withdrawal of this § 103 (a) rejection is respectfully requested.

Claims 16-17 and 19-25 depend either directly or indirectly from amended claim 15, and include all the features of claim 15, plus additional features that are not discussed or suggested by the references relied upon. Therefore, claims 16-17 and 19-25 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

For reasons similar to those discussed above, neither Yamada nor Iwata discusses or suggests "a conversion circuit that, based on a state of the flag, converts an address indicating a nonvolatile storage place of an interrupt vector that is accessed by the central processing unit into an address indicating a nonvolatile storage place of a corresponding alternate interrupt vector," as recited in claim 29 as amended. Therefore, claim 29 patentably distinguishes over the references relied upon. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

In the Office Action, at pages 8-12, numbered paragraphs 15-24, claims 1, 4, and 6-12 were rejected under 35 USC § 103(a) as being unpatentable over Yamada in view of Iwata and further in view of Hashimoto (U.S. Patent No. 6,654,839).

For reasons similar to those discussed above, neither Yamada nor Iwata, nor the combination thereof, discusses or suggests "a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address," as recited in amended claim 1. Hashimoto fails to make up for this deficiency in Yamada and Iwata. Specifically, Hashimoto does not discuss or suggest "a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address," as recited in claim 1. Therefore, claim 1 patentably distinguishes over Yamada, Iwata, and Hashimoto, and any combination thereof. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Claims 4 and 6-12 depend either directly or indirectly from amended claim 1, and include all the features of claim 1, plus additional features that are not discussed or suggested by the references relied upon. Therefore, claims 4 and 6-12 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

In the Office Action, at pages 12-15, numbered paragraphs 25-26, claim 28 was rejected under 35 USC § 103(a) as being unpatentable over Yamada in view of Iwata and further in view of Yoshioka et al. (U.S. Patent No. 6,038,661).

For reasons similar to those discussed above, neither Yamada nor Iwata, nor the combination thereof, discusses or suggests "a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by adding the offset to

the first address," as recited in amended claim 28. Yoshioka et al. fails to make up for this deficiency in Yamada and Iwata. Specifically, Yoshioka et al. does not discuss or suggest "a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by adding the offset to the first address," as recited in claim 28. Therefore, claim 28 patentably distinguishes over Yamada, Iwata, and Hashimoto, and any combination thereof. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

In the Office Action, at pages 15-19, numbered paragraphs 27-34, claims 5, 13-14, 18, and 26-27 were rejected under 35 USC § 103(a) as being unpatentable over Yamada in view of Iwata and further in view of various other combinations of prior art.

Claims 5 and 13-14 and claims 18 and 26-27 depend either directly or indirectly from claims 1 and 15, respectively, and include all the features of claims 1 and 15, plus additional features that are not discussed or suggested by the references relied upon. Therefore, claims 5, 13-14, 18, and 26-27 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

CONCLUSION

Claims 1 and 4-29 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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